AMERICAN UNIVERSITY
OF CYPRUS

Course Code	Course Name	ECTS Credit
CSC301	Computer Architecture II	7.5
Pre-Requisite	**Course Type**	**Language of Instruction**
CSC202	Compulsory	English
Year of Study	**Level of Course**	**Mode of Delivery**
3rd / 5th	BSc/1st Cycle	On Campus

Course Objectives:

To introduce students to the computer architecture and organization with emphasis on performance metrics and cost, instruction set architectures, RISC processor design, pipelining, and memory hierarchy.

Learning Outcomes

By the end of this course students should:

- Understand the computer architecture and organization of modern processors.
- Describe and analyze the ISA of high performance processors with respect to their need and instruction formats, and use a given ISA to develop programs in assembly language
- Evaluate the performance of computer systems using performance metrics such as CPI, IPC, AS well as hardware cost and power requirements.
- Design a single-cycle and a multi-cycle datapath as well as the control unit of a typical RISC processor.
- Explain the design of a modern pipelined datapath and apply hardware optimizations such as data forwarding, branch prediction etc, as well as software optimizations such as loop unrolling.
- Analyse and evaluate the memory hierarchy of a modern computer, including cache architectures and virtual memory, and employ optimizations such as prefetching, multilevel caches and victim caches that improve the performance of the computer.
- Further advance their knowledge in designing computer architecture systems using Assembly, C/C++ and VHDL.

Teaching Methodology:

In the Classroom: Lecturers make use of whiteboards, flipcharts, overhead projector, video material and power point presentations. Students are supplied with handouts on extra or relevant material. One personal Computer Labs equipped with Multimedia PCs of the latest technology with the required software, scanners, printers and

LCD-Projectors, satisfy the classes' requirements. All PCs are connected to the Internet, through a Broad Band High speed permanent connection using cable technology.

Web Supported Learning: All the teaching material and the Lecturer's presentations are uploaded on the electronic learning platform of the college as a supporting studying tool.

Guest Speakers / Visits: External visits to agencies or relevant industry/subject related organizations are arranged. Guest speakers that are experts in their field are invited to address the students. Students are also encouraged to visit industry players and familiarize themselves with the profession they have chosen.

Teaching Methods: Lectures, presentations, videos, problem and case study discussion, discussion on relevant articles, independent and private study, preparation of projects, fieldwork and group work.

Course Content

- **Introduction to Computer Architecture:** Organisation and abstraction of a computer. ISAs. Emerging computer architecture technologies. Processor, caches, memory and I/O devices.

- **Performance Metrics:** Measuring performance and metrics. Improve performance, clock cycles, CPI, instructions count, MIPS, MOPS, MFLOPs. Benchmarks. Amdahl's Law.

- **Instruction Set Architecture (ISA):** Specifications, classes, registers, memory addressing and addressing modes. The complete MIPS architecture and in-depth analysis. The 80*86 and Pentium 4 processors. Compilers and ISAs.

- **RISC Processor Design:** Full ALU design of the MIPS processor. Multiplication and division algorithms in hardware. Single-cycle, multi-cycle datapath and controller design.

- **Pipelining**: Single-cycle, Multi-cycle versus Pipeline. Structural, data and control hazards. Forwarding. Exceptions. MIPS R3000 pipeline and design of a pipelined processor. Loop unrolling in scalar and superscalar computer systems. Software pipelining.

- **Memory Hierarchy**: Locality and memory hierarchy. SRAM and DRAM. Memory organization. Advanced cache memory. Virtual memory. Protection. Translation Lookaside Buffer (TLB).

- **Laboratory Work**: Individual or small group experiments performed with the use of common FPGA boards and VHDL. Experiments include the design and analysis of advanced CPUs.

Assessment Methods:

The final course grade is made up of:

Coursework

Final Examination

Final Examination marks constitute 60% of the final semester mark, while Midterm Examinations and assignments (when applicable) constitute the 40% and participation,

The pass mark is set at 50%

The Midterm examinations are based on material covered during a given period and are set towards the end of November in the case of Fall semesters, the end of March in the case of Spring semesters, and the end of July in the case of summer sessions.

These take place during lesson time and take no more than two study periods to complete.

Final examinations are based on material covered throughout the semester. The dates for these are set down on the academic calendar. The Final Examinations have duration of three hours for Diplomas, Bachelor Degrees and Master Degrees.

Final examination marks are combined with the marks from the Midterm examinations, participation and assignments (when applicable) to produce the final mark for the semester.

Required Textbooks/Reading:

Title	**Author(s)**	**Publisher**	**Year**
Computer Organization and Design MIPS Edition: The Hardware / Software Interface	David A Patterson and John L Hennessy	Morgan Kaufmann Publishers / 2020	2020
Introduction to Logic Circuits & Logic Design with VHDL	Brock J. LaMeres	Springer/2019	2019
Laboratory Manual	George Dekoulis	AUCY 2020	2020

Recommended Further Bibliography:

Title	**Author(s)**	**Publisher**	**Year**
Logic and Computer Design Fundamentals	M. Mano	Pearson International /2015	2015
Introduction to Digital Design Using Digilent FPGA Boards	Richard E. Haskell and Darrin M. Hanna	LBE Books / 2019	2019
Designing with Xilinx FPGAs: Using Vivado	Sanjay Churiwala	Springer/2017	2017
Digital Design Using Digilent FPGA Boards: VHDL / Vivado Edition	Richard E. Haskell and Darrin M. Hanna	LBE BOOKS/2019	2019
Digital Electronics with DIGILENT BASYS 2 & 3 FPGA Boards: Implementation of Combinational and Sequential Logic Circuits using Digilent BASYS 2 & BASYS 3 Boards with Xilinx FPGAs	Andrzej J. Gapinski	LAP/2018	2018